In the Claims:

Please cancel claims 1 and 5 without prejudice or dedication.

1. (cancelled)

2. (currently amended) A ~~The~~ method for direct access to bit fields in instruction operands ~~according to claim 1~~, further comprising:

providing indications of bit fields in source and target operands of a processor executable instruction, each of the indicated bit fields consisting of a plurality of bits in a plurality of bit positions in the source and target operands;

performing the processor executable instruction utilizing the bit fields in the source and target operands in response to the indications of the bit fields ; and

providing, by performing the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands;

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator;

wherein no instruction depends on a preceding instruction because each instruction in a pipeline is executed for a different thread.

3. (currently amended) The method for direct access to bit fields in instruction operands according to claim 2~~1~~, further comprising:

transferring the data after modifying and forwarding to an output buffer.

4. (currently amended) The method for direct access to bit fields in instruction operands according to claim 2~~1~~, further comprising:

processing data at a rate of at least 10 Gbs.

5. (cancelled)

5. (previously presented) An apparatus for directly accessing bit fields in instruction operands, said apparatus comprising:

at least one memory;

at least one processor;

a bus interconnecting said at least one memory and said at least one processor;

wherein one of said at least one processor retrieves indications of bit fields, said bit fields each consisting of a plurality of bits in a plurality of bit positions within the source and target operands for a processor executable instruction, performs the processor executable instruction utilizing the bit fields in said source and target operands in response to the indications of the bit fields, and provides, by performance of the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands.

6. (currently amended) An ~~The~~ apparatus for directly accessing bit fields in instruction operands ~~according to claim 5~~, comprising ~~wherein said processor comprises~~:

at least one memory;

at least one processor;

a bus interconnecting said at least one memory and said at least one processor;

wherein one of said at least one processor retrieves indications of bit fields, said bit fields each consisting of a plurality of bits in a plurality of bit positions within the source and target

operands for a processor executable instruction, performs the processor executable instruction utilizing the bit fields in said source and target operands in response to the indications of the bit fields, and provides, by performance of the processor executable instruction, and in response to the indications of the bit fields, direct manipulation of any bits in any bit field of the source and target operands; and

wherein the processor comprises:

an analysis machine having multiple pipelines,;

a packet task manager operationally connected to said analysis machine,; and,

a packet manipulator operationally connected to said analysis machine.

7. (original) The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

8. (original) The apparatus according to claim 6, wherein said analysis machine has 32 threads.

9. (previously presented) The apparatus according to claim 6, further comprising:

a packet task manager operationally connected to said analysis machine;

a packet manipulator operationally connected to said analysis machine; and

a global access bus including a master request bus and a slave request bus separated from each other and pipelined.

10. (original) The apparatus according to claim 6, further comprising:

an external memory engine operationally connected to said analysis machine; and

a hash engine operationally connected to said analysis machine.

11. (original) The apparatus according to claim 9, further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine.

12. (original) The apparatus according to claim 9, further comprising:

packet data global access bus software code used for flow of packet data between a flexible data input bus and a packet manipulator.

13. (original) The apparatus according to claim 9, further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator.

14. (original) The apparatus according to claim 9, further comprising:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

15. (original) The apparatus according to claim 9, further comprising:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

16. (original) The apparatus according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

17. (canceled)

18. (original) The apparatus according to claim 9, further comprising:

a bi-directional access port operationally connected to said analysis machine;

a flexible data input buffer operationally connected to said analysis machine; and

a flexible data output buffer operationally connected to said analysis machine.